Amendments to the Specification

Kindly amend paragraph [0140] appearing at page 9 and continuing on page 10, to read as follows:

[0140] ~~When the input signal D shifts from a state of high level to a state of low level~~ In the state that the input signal D and the output signal Q are a state of high level, if the input signal D goes to a state of low level, output signal Q goes to a low level, the second transmission gate TG22 of the comparing circuit 430 turns on, and the third transmission gate TG23 turns off. As the signal at the third node N3 of the latch 420 still maintains a high level and the signal at the fourth node N4 is at a low level, the second transmission gate TG22 transfers the low-level signal to the sixth node N6. As the signal of the seventh node N7 goes to a high level, the fourth transmission gate TG24 turns on and the PMOS transistor MP1 turns off. Accordingly, the external clock signal CLK, and the external clock signal CLKB delayed and inverted by the delay circuit 444, are applied to the NAND gate 442. At this time, the output signal of the internal clock generating circuit 440 is configured to be a pulse signal with a pulse width smaller than that of the external clock signal CLK. When the external clock signal CLK shifts from a low level to a high level, the rising edge of the output signal of the NAND gate 442 is provided. When the external clock signal CLKB delayed by the delay circuit 444 shifts from a high level to a low level, the falling edge of the output signal of the NAND gate 442

is formed. The output signal of the NAND gate 442 acts as the inverted internal clock signal CKN, and the output of the clock buffer 410 formed with the inverter INV32 acts as the internal clock signal CK. Fig. 5 is a timing diagram illustrating the process of generating the internal clock signal.